UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/743,079 | 12/23/2003 | Uming Ko | TI-29632.1 | 8111 |

23494 7590 02/27/2006

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

| EXAMINER | |
|---|---|
| FARAHANI, DANA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2891 | |

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/743,079 | KO, UMING | |
| | Examiner | Art Unit | |
| | Dana Farahani | 2891 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-23-03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5, 15, 26, and 36 are rejected under 35 USC 112 ,second paragraph for failing to convey to one of ordinary skill in the art the bounds of those claims. Specifically, it is not clear as to what is meant by "Complementary" output buffer. The word complementary has more than one definition in the art, in the field of integrated circuits and semiconductors, and one of ordinary skill in the art cannot determine from the disclosure of the instant application the exact definition of "complementary" output buffer.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the

reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2, 4, 6, 8-10, 22, 23, 25, 27, and 29-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al., hereinafter Sato (US Patent 6,388,857).

Regarding claims 1, 2, 22, and 23, Sato discloses in figures 4 and 7 a bond pad 5 formed on a substrate;

an electrostatic discharge device 24 formed in the substrate, the electrostatic discharge device being at least partially formed beneath the bond pad;

an I/0 buffer 22 formed in the substrate and connected to the bond pad, the I/0 buffer providing communication between the bond pad and circuitry formed in the substrate, wherein the circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/0 buffer, as can be seen in the figures.

Regarding claims 4 and 25, the buffer is an input buffer.

Regarding claims 6 and 27, the circuitry is CMOS circuitry (see col. 8, lines 61-62).

Regarding claims 8, 9, 29, and 30, the circuitry is an application specific integrated circuit and also digital signal processor (it is a memory circuitry).

Regarding claims 10 and 31, the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

*Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 12, 14, 16, 18, 19-21, 32, 33, 35, 37, and 39-41 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Sato.

Regarding claims 11, 12, 32, and 33, Sato discloses an integrated circuit comprising:

a functional core 23 formed on a substrate, the functional core, at least the region II thereof being positioned centrally on the substrate; and

an I/0 region 23 positioned at the periphery of the functional core, the I/0 region including an I/0 module, the I/0 module including:

a bond pad 5 formed on a substrate;

an electrostatic discharge device 24; and

an I/0 buffer 22 wherein the I/0 buffer is not positioned between the bond pad and the functional core. Note that also Sato does not explicitly disclose a plurality of I/O modules, semiconductor devices are normally mass-produced for cost saving purposes.

Regarding claims 14 and 35, the buffer is an input buffer.

Regarding claims 16, 21, and 37, the circuitry is CMOS circuitry (see col. 8, lines 61-62).

Regarding claims 18, 19, 39, and 40, the circuitry is an application specific integrated circuit and also digital signal processor (it is a memory circuitry).

Regarding claims 20 and 41, the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

7. Claims 3, 13, 24, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato as applied to claim 1, 11, 22, and 32 above, and further in view of Tobita (US Patent 4,980,799).

Sato discloses the claimed invention, as discussed above, except for the I/O buffer is an output buffer.

Tobita discloses that an output buffer is provided for a memory module to be used in a memory array (see figure 1, and column 1, lines 50-56). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an out put buffer fore the memory circuit of the structure of Sato in order to make the output data suitable for read out in an application of the memory module.

8. Claims 7, 17, 28 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato as applied to claims 1, 11, 22, and 32 above, and further in view of Kim et al., hereinafter Kim (US Patent 5,989,968).

Sato discloses the claimed invention, as discussed above, except for the circuitry is BICMOS circuitry.

Kim discloses that in a memory cell, it is known to implement a BICMOS structure for their low current consumption and high operational speed (see figure 1; and column 1, lines 14-15 and 27-36). Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention to use the structure of the Sato reference such that the memory module therein implements a BICMOS structure, since it is well known in the art that those structures are advantageously used in memory modules for their low power consumption and high speed.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800